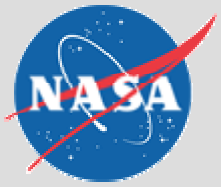


Scaling, Packaging and Testability

Or

No, They're Not Packaging the Parts That Way Just to P&#! You Off

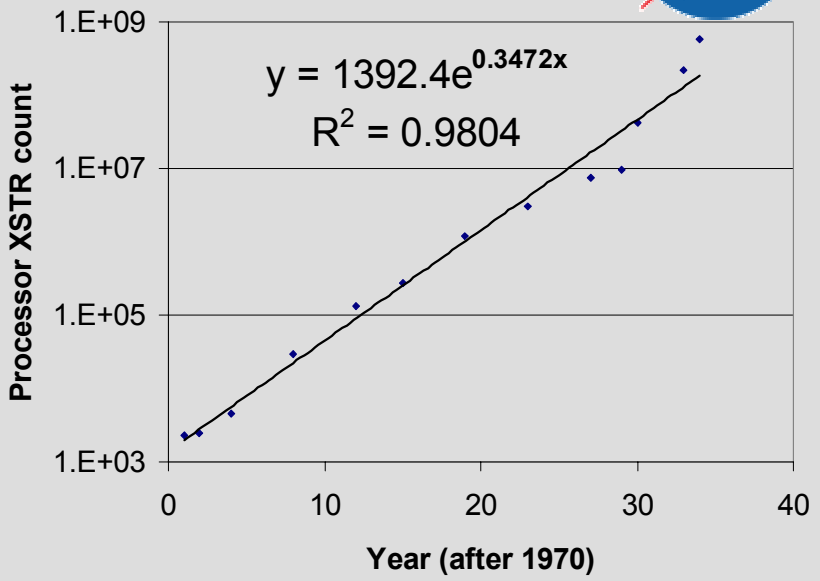
Ray Ladbury

GSFC Radiation Effects and Analysis Group

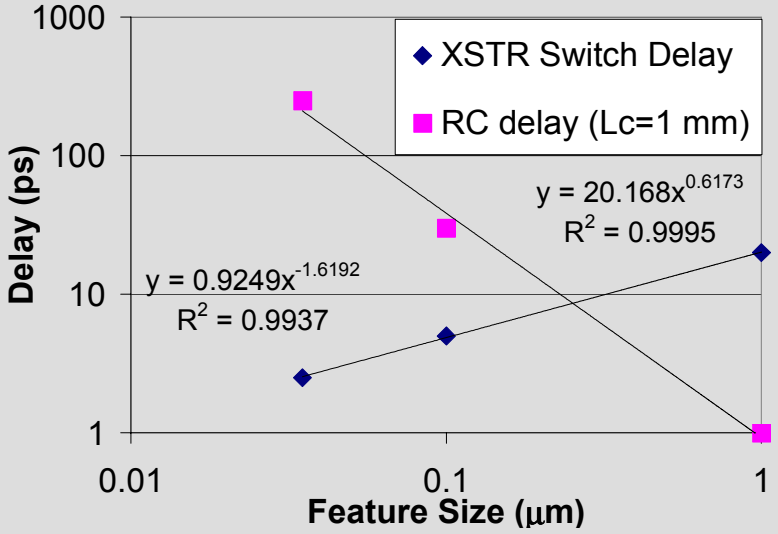
The author would like to acknowledge the sponsorship of the NASA Electronic Parts and Packaging Program.

Packaging: The Rodney Dangerfield of Electronics

- Scaling continues apace and garners most of the headlines. However, the front lines of the battle for greater integration, speed and density have shifted.
  - Increased scaling may not bring greater speed

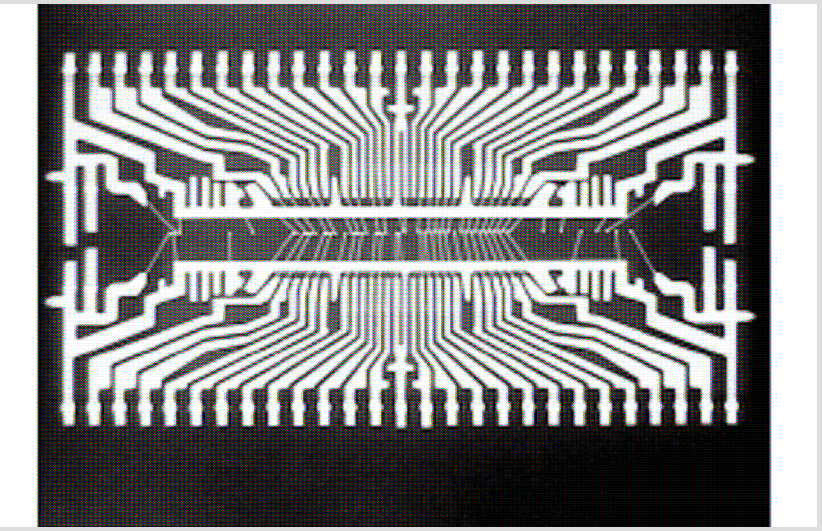


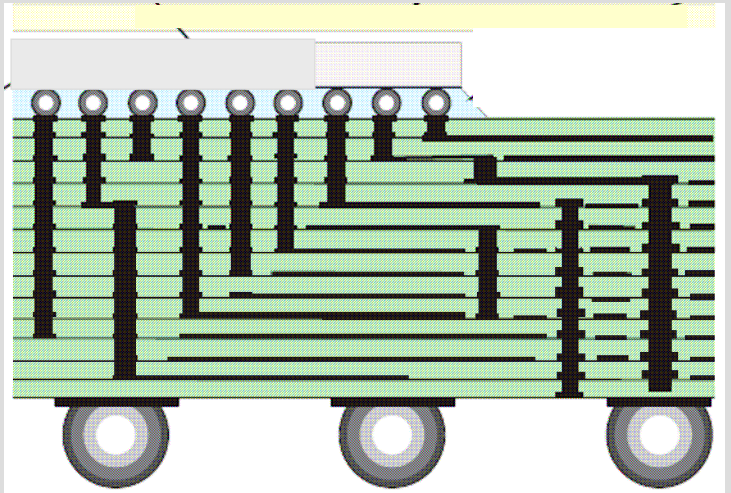
- Packaging/interconnects now critical
  - Limiting factor for speed
  - Thermal issues
  - Critical functions (e.g. PLLs)
  - Cost rise projected ~5% per pin
- Why care?
  - Packaging affects testability



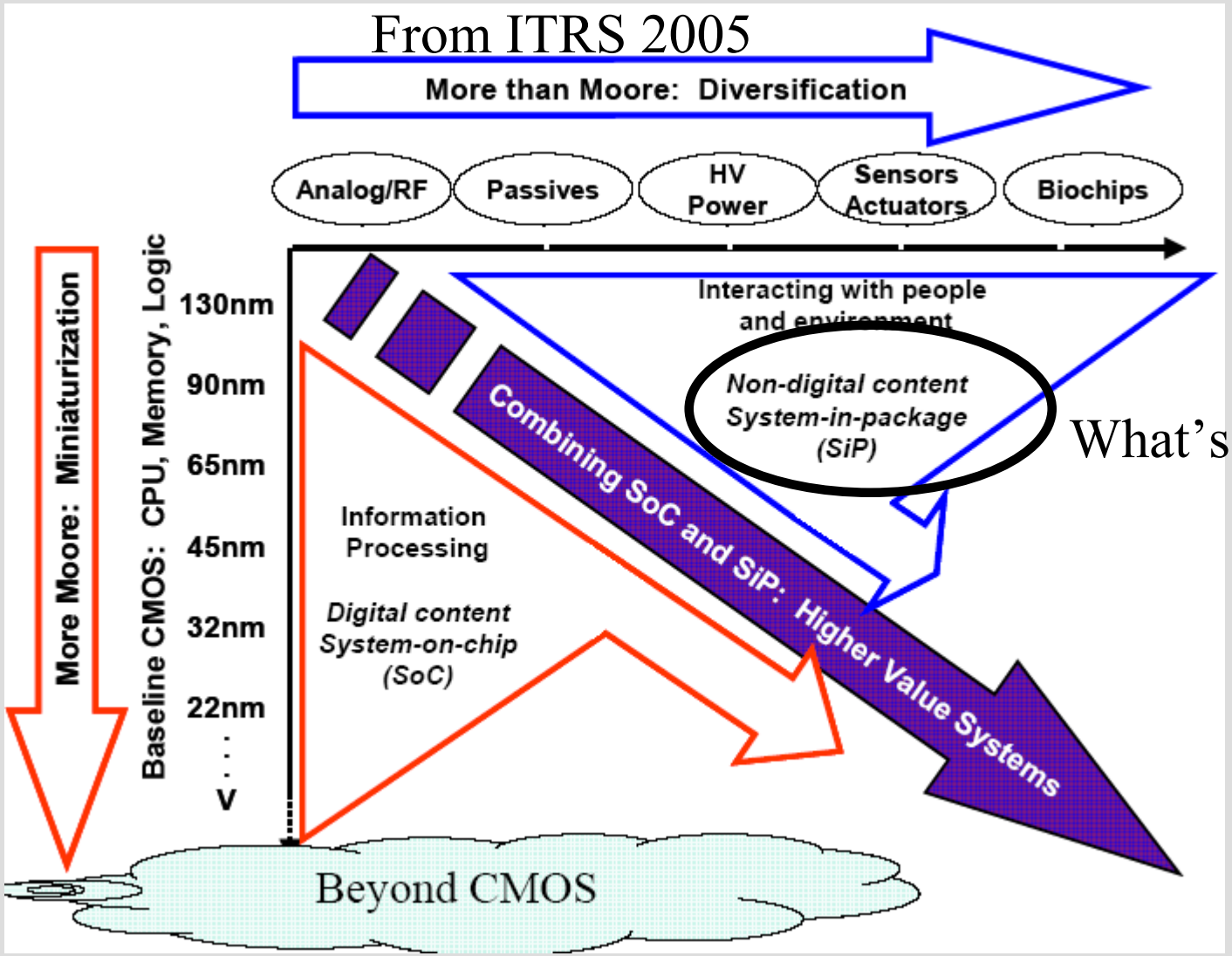
Packaging Issues and Testability: Not New

- Packaging issues are not new
  - Metal lead frames for DRAMs limit bondwire lengths
  - Flip-chip packages provide the shortest interconnects for high speed
- Traditional test prep strategies:
  - Repackaging
  - Die thinning/backside irradiation
  - Ultrahigh-energy heavy-ion (UEHI) beams
  - Proton testing to infer HI behavior
  - All these strategies pose difficulties
    - Yield
    - Fidelity/interpretation of results



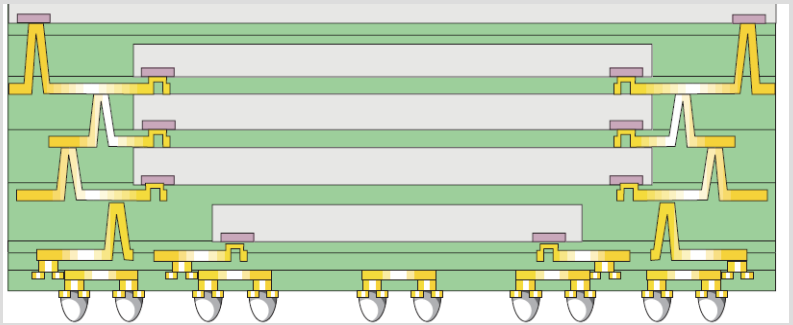


So, where is packaging headed next?

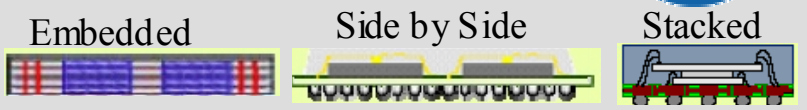


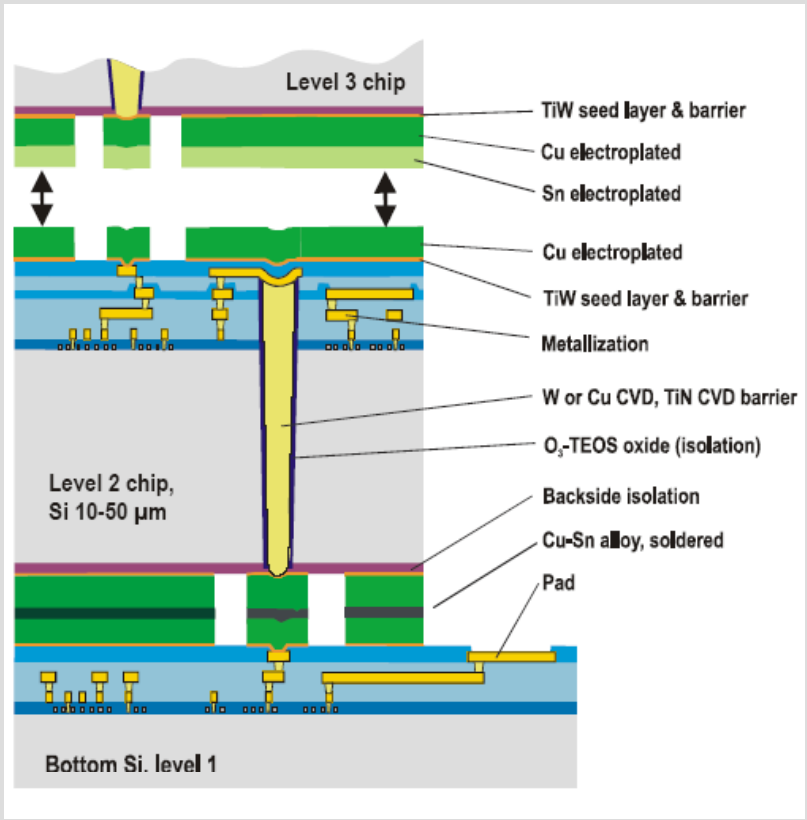
*lifted shamelessly from ITRS-2005, Executive Summary

System in a Package (SiP)—Why?



- Allows close integration of many different technologies
  - CMOS, analog RF, sensors…
- Provides shortest interconnects
- Can alleviate thermal issues
- Optimizes weight and space
- Offers a path to increased integration even if scaling fails
- But How do you test it?

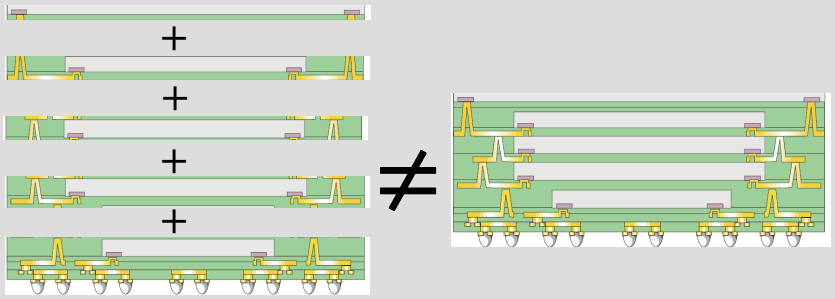




*adapted from ITRS-2005, Assembly and Packaging

Repackaging and Backside Irradiation

- Repackaging could be promising
  - Best strategy: Obtain pkg'd die
  - Repackaging problematic
    - thinned die→poor yield
  - No guarantee that system will perform as the sum of its parts.
    - Need high-fidelity simulation to drive each chip
  - Even if repackaging works
    - Weakest link drives performance
    - Can't current limit for SEL

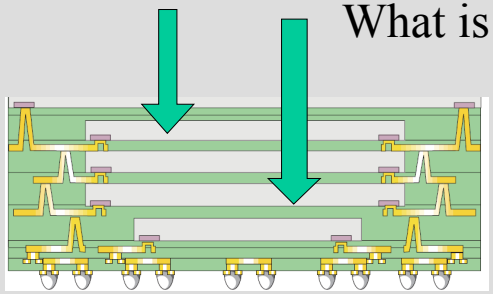


- Thinning and backside irradiation
  - Work well for monolithic chips
    - Preserves interconnects, timing
    - Main issue is affecting diffusion-related charge collection
  - Will not work for SiP
    - Note this means two-photon absorption also not feasible
  - However
    - Die usually thinned (10-50 μm) by mfg to limit package thickness
    - If individual die are obtainable and function properly
      - May be able to irradiate from front or backside
      - TPA may work just fine
    - Problem reduces to the same as that for repackaging.

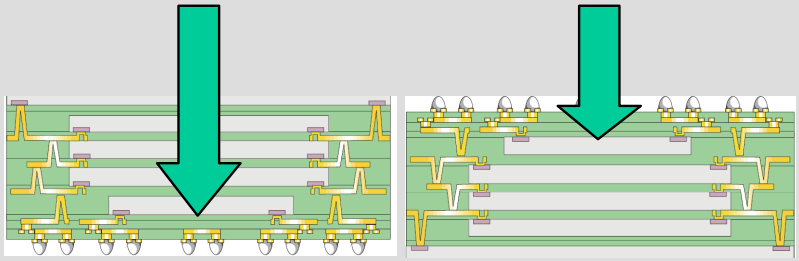
Ultra-high Energy Heavy Ion Irradiation

- If energies sufficiently high, ion beam may penetrate entire package.
  - Stimulates all possible error modes under realistic operating conditions
  - If secondary effects are important, energy range of ions is more similar to space radiation environment
  - Unfortunately, interpreting results may not be trivial.
    - Ions traverse several layers and LET of ion changes as it loses energy.
    - Similar uncertainties occur when a lead frame covers part of die.

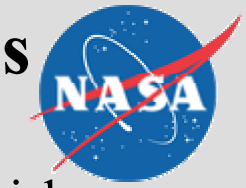
What is ion LET?



- Possible solutions
  - Use VERY high-energy (minimum ionizing) ions
  - Degrade beam energy until error mode stops.
  - Compare results for front and backside irradiation over angles
  - All these solutions are time consuming and beam time at high-energy facilities is expensive
    - Simulation may help in interpreting results if sufficient design info available

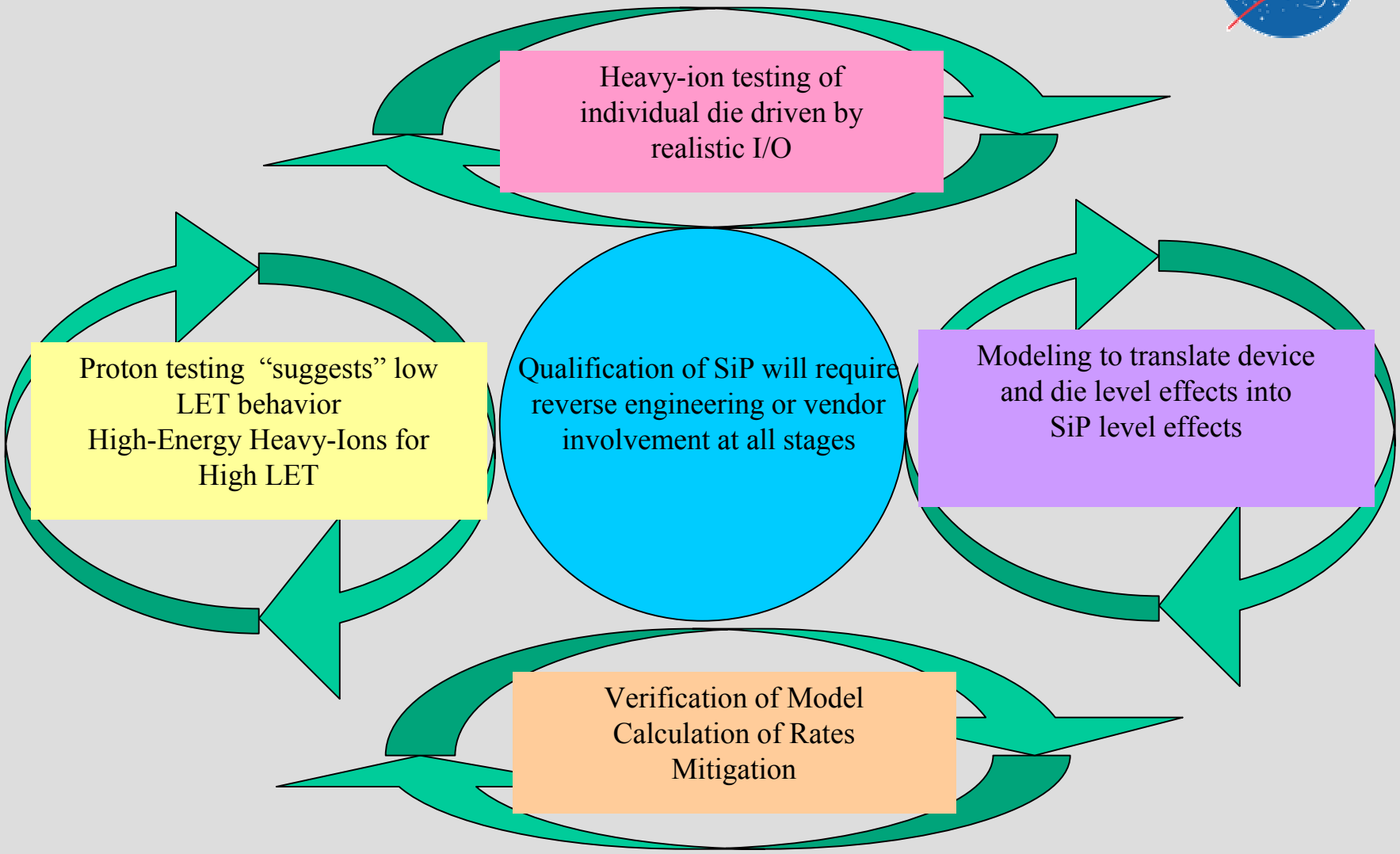


Extrapolating from Protons to Heavy Ions



- Proton-induced upsets in ICs caused by heavy ions recoiling from proton collision
  - In some cases, can infer limited information about heavy-ion response from proton data
    - max LET of recoils is 12-15 MeVcm^2/mg
  - Protons have good penetration
  - Testing can even be done for full commercial electronic systems
  - Beam time at proton facilities is relatively cheap
  - For some devices and environments, protons may dominate upset rates
- Such extrapolations carry risk
  - Some devices exhibit SEE for low LET ions but not for protons
  - Low proton interaction cross section
    - means parts may see high TID in proton testing
  - Proton testing can be complicated
    - Inelastic and elastic scattering
    - High Z recoils
    - Angle effects
  - Short recoil range may not reproduce heavy-ion effects
  - Proton testing generally not adequate to ensure hardness for most missions
  - Extrapolating from protons to heavy ions can be misleading

Qualification Suggestions



Qualification Suggestions II

UEHI Testing Issues

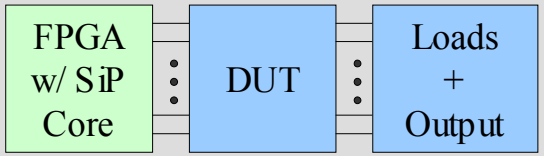
- Energy tuning is important
  - Changing energy changes LET
  - ID die an error mode occurs in
  - Only way to test the whole SiP

Proton Issues and Caveats

- Goal is to infer low-LET heavy ion behavior as well as proton behavior
  - Proton $\sigma \sim 10^{-6}$ heavy ion σ (TID an issue)
  - Method is not 100% reliable
  - High Z recoils and angle effects may occur

Testing Individual Die

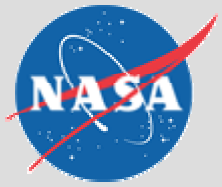
- Each die tested needs realistic I/O
  - Board Layout/Signal Integrity Crucial
  - FPGA controller is promising
    - Core needs to be high fidelity



Getting to an Answer

- LET determination for high-energy, heavy ions is uncertain
  - Live with it or test individual die
- Seeing proton SEE→Low onset LET
  - Absence of SEE ↛High onset LET
- Proton + UEHI testing may give a rough estimate of SEE behavior
- Need more accuracy?
  - Irradiate individual die
  - Model SiP- inject errors from each die
  - Verify by showing model explains all modes seen during UEHI test

Conclusions



- Even if Scaling tapers off, integration of electronics will continue
  - SiP is a new frontier—integration of dissimilar semiconductor technologies
- SiP are very attractive for space flight
  - Small footprint, low weight, high-performance
  - A single chip may replace a box
    - With only 500 kg of gear for crew on lunar missions, that's tempting
- SiP may pose unprecedented challenges to radiation qualification
  - Package is specially engineered to optimize performance
    - Interconnects are minimized to optimize timing, signal integrity and integration
    - Package also helps with structural support (for thinned die) and thermal issues
  - Qualification may involve UEHI and proton testing, modeling and verification
    - Involvement of vendors is highly desirable and probably essential
    - It won't be cheap!!!
- Will the cost and/or risk will be too high for future programs?
  - Know anyone who's taking bets?